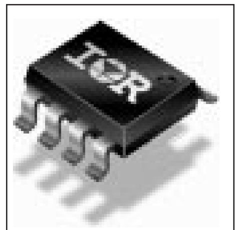
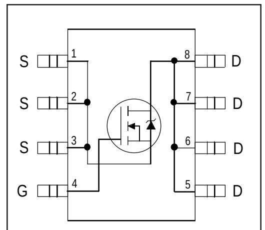
International
IOR Rectifier

PD-94009

IRF7811AV

- N-Channel Application-Specific MOSFETs
- Ideal for CPU Core DC-DC Converters
- Low Conduction Losses
- Low Switching Losses
- Minimizes Parallel MOSFETs for high current applications


SO-8



Top View

Description

This new device employs advanced HEXFET Power MOSFET technology to achieve an unprecedented balance of on-resistance and gate charge. The reduced conduction and switching losses make it ideal for high efficiency DC-DC converters that power the latest generation of microprocessors.

The IRF7811AV has been optimized for all parameters that are critical in synchronous buck converters including $R_{DS(on)}$, gate charge and Cdv/dt-induced turn-on immunity. The IRF7811AV offers an extremely low combination of Q_{sw} & $R_{DS(on)}$ for reduced losses in both control and synchronous FET applications.

The package is designed for vapor phase, infra-red, convection, or wave soldering techniques. Power dissipation of greater than 2W is possible in a typical PCB mount application.

DEVICE CHARACTERISTICS⑤

	IRF7811AV
$R_{DS(on)}$	11mΩ
Q_G	17nC
Q_{sw}	6.7nC
Q_{oss}	8.1nC

Absolute Maximum Ratings

Parameter		Symbol	IRF7811AV	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain or Source	T_A = 25°C	I_D	10.8	
Current ($V_{GS} \geq$ 4.5V)	T_L = 90°C		11.8	A
Pulsed Drain Current①		I_{DM}	100	
Power Dissipation③	T_A = 25°C	P_D	2.5	W
	T_L = 90°C		3.0	
Junction & Storage Temperature Range		T_J, T_{STG}	–55 to 150	°C
Continuous Source Current (Body Diode)		I_S	2.5	A
Pulsed Source Current①		I_{SM}	50	

Thermal Resistance

Parameter		Max.	Units
Maximum Junction-to-Ambient③	$R_{\theta JA}$	50	°C/W
Maximum Junction-to-Lead	$R_{\theta JL}$	20	°C/W

12/13/00

Electrical Characteristics

Parameter		Min	Typ	Max	Units	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSS}	30	–	–	V	V_{GS} = 0V, I_D = 250µA
Static Drain-Source on Resistance	$R_{DS(on)}$		11	14	mΩ	V_{GS} = 4.5V, I_D = 15A②
Gate Threshold Voltage	$V_{GS(th)}$	1.0			V	V_{DS} = V_{GS}, I_D = 250µA
Drain-Source Leakage Current	I_{DSS}			20	µA	V_{DS} = 24V, V_{GS} = 0
				100	µA	V_{DS} = 24V, V_{GS} = 0, Tj = 100°C
Gate-Source Leakage Current	I_{GSS}			±100	nA	V_{GS} = ±20V
Total Gate Chg Cont FET	Q_G		17	26	nC	V_{GS}=5V, I_D=15A, V_{DS}=24V
Total Gate Chg Sync FET	Q_G		14	21	nC	V_{GS} = 5V, V_{DS}< 100mV
Pre-Vth Gate-Source Charge	Q_{GS1}		3.4		nC	V_{DS} = 16V, I_D = 15A
Post-Vth Gate-Source Charge	Q_{GS2}		1.6		nC	
Gate to Drain Charge	Q_{GD}		5.1		nC	
Switch Chg(Q_{gs2} + Q_{gd})	Q_{sw}		6.7		nC	
Output Charge	Q_{oss}		8.1	12	nC	V_{DS} = 16V, V_{GS} = 0
Gate Resistance	R_G		2.2		Ω	
Turn-on Delay Time	$t_{d\ (on)}$		8.6		ns	V_{DD} = 16V, I_D = 15A
Rise Time	t_r		21		ns	V_{GS} = 5V
Turn-off Delay Time	$t_{d\ (off)}$		43		ns	Clamped Inductive Load
Fall Time	t_f		10		ns	
Input Capacitance	C_{iss}	–	1801	–	pF	V_{DS} = 16V, V_{GS} = 0
Output Capacitance	C_{oss}	–	723	–	pF	
Reverse Transfer Capacitance	C_{rss}	–	46	–	pF	

Source-Drain Rating & Characteristics

Parameter		Min	Typ	Max	Units	Conditions
Diode Forward Voltage	V_{SD}			1.3	V	I_S = 15A②, V_{GS} = 0V
Reverse Recovery Charge④	Q_{rr}		50		nC	di/dt ~ 700A/µs V_{DS} = 16V, V_{GS} = 0V, I_S = 15A
Reverse Recovery Charge (with Parallel Schottky)④	$Q_{rr(s)}$		43		nC	di/dt = 700A/µs (with 10BQ040) V_{DS} = 16V, V_{GS} = 0V, I_S = 15A

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.
② Pulse width ≤ 400 µs; duty cycle ≤ 2%.
③ When mounted on 1 inch square copper board, t < 10 sec.
④ Typ = measured - Q_{oss}
⑤ Typical values of R_{DS}(on) measured at V_{GS} = 4.5V, Q_G, Q_{SW} and Q_{OSS} measured at V_{GS} = 5.0V, I_F = 15A.

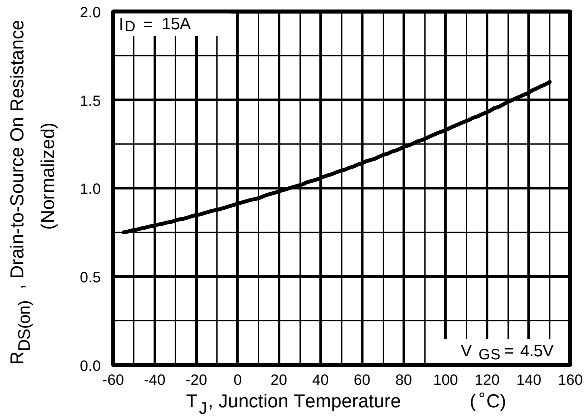


Figure 1. Normalized On-Resistance vs. Temperature

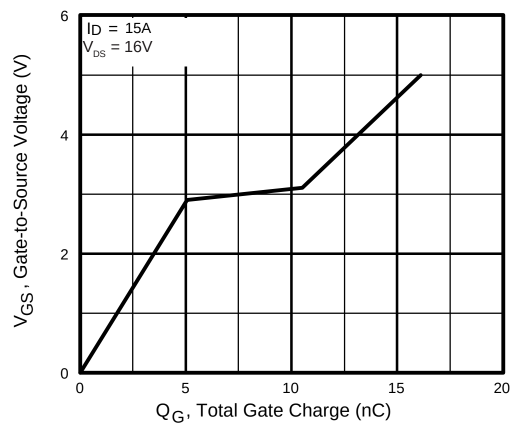


Figure 2. Gate-to-Source Voltage vs. Typical Gate Charge

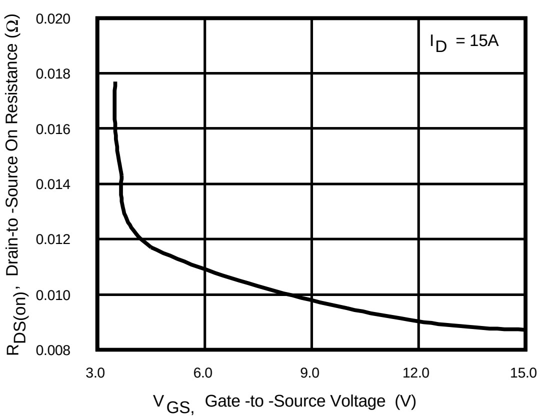


Figure 3. Typical Rds(on) vs. Gate-to-Source Voltage

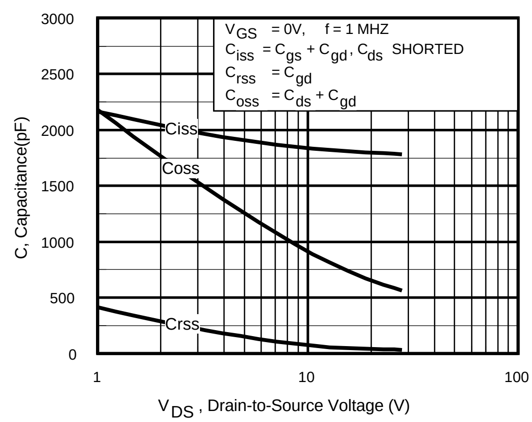


Figure 4. Typical Capacitance vs. Drain-to-Source Voltage

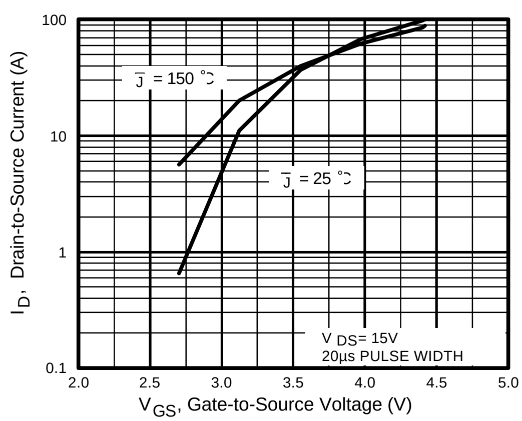


Figure 5. Typical Transfer Characteristics

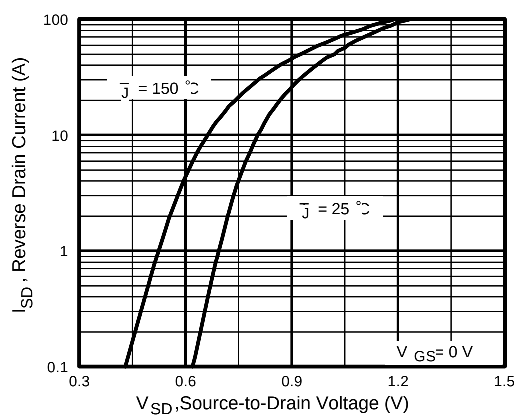


Figure 6. Typical Source-Drain Diode Forward Voltage

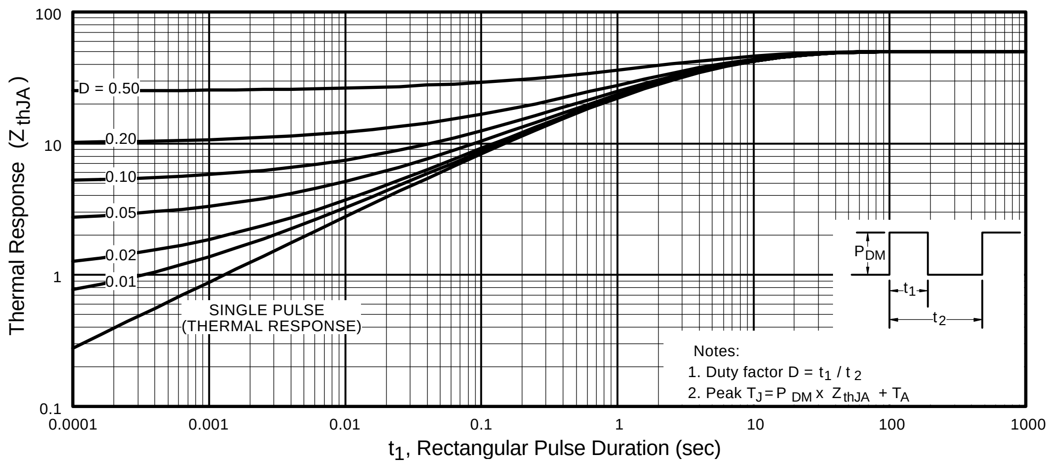


Figure 7. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

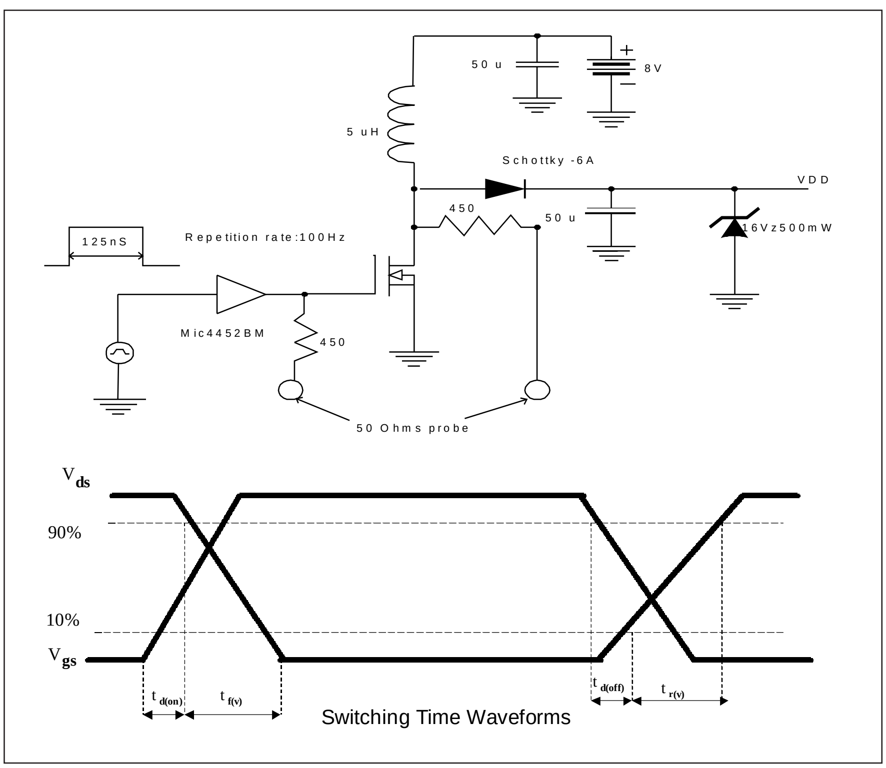
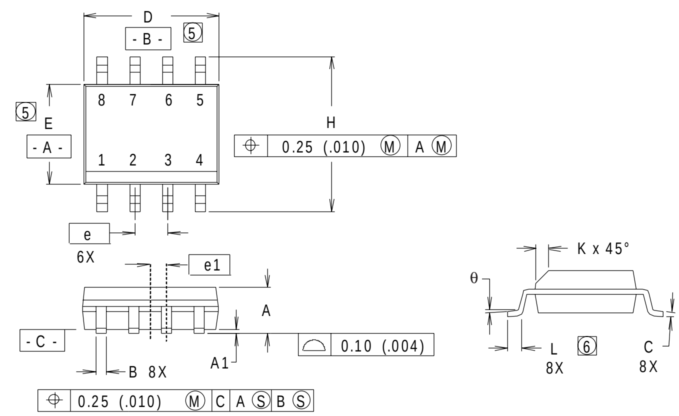


Figure 8. Clamped Inductive load test diagram and switching waveform

SO-8 Package Details



NOTES:

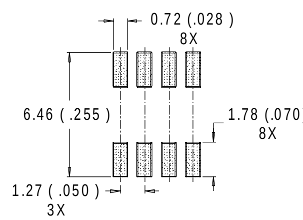
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION : INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.006).

6 DIMENSIONS IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE..

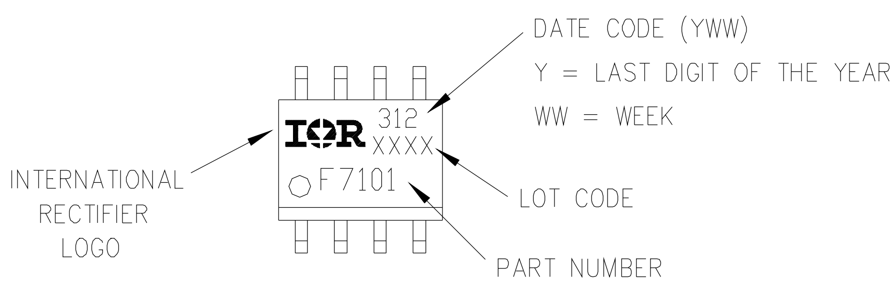
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	0.16	.050	0.41	1.27
θ	0°	8°	0°	8°

RECOMMENDED FOOTPRINT

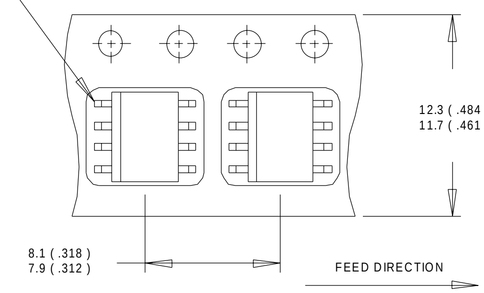


SO-8 Part Marking

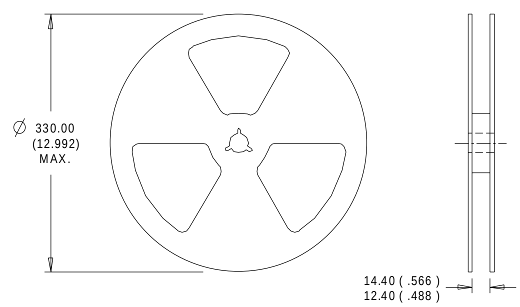
EXAMPLE: THIS IS AN IRF7101



SO-8 Tape and Reel



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
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Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web site.

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