



STB9NK90Z - STFPNK90Z STP9NK90Z - STW9NK90Z

N-channel 900V - 1.1Ω - 8A - TO-220 /FP- D²PAK - TO-247
Zener-protected superMESH™ MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D	P _w
STB9NK90Z	900V	<1.3Ω	8A	160 W
STW9NK90Z	900V	<1.3Ω	8A	160 W
STP9NK90Z	900V	<1.3Ω	8A	160 W
STF9NK90Z	900V	<1.3Ω	8A	160 W

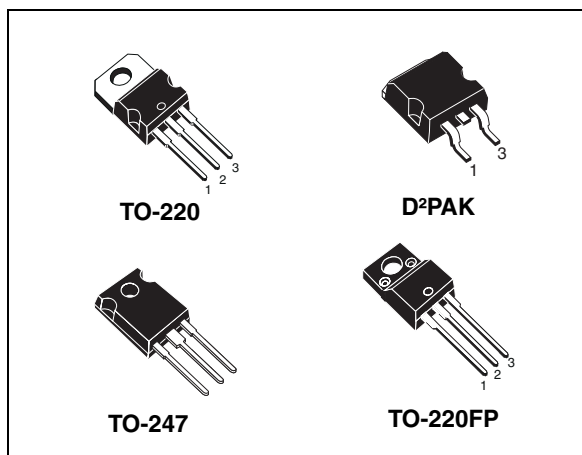
- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized

Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications.

Applications

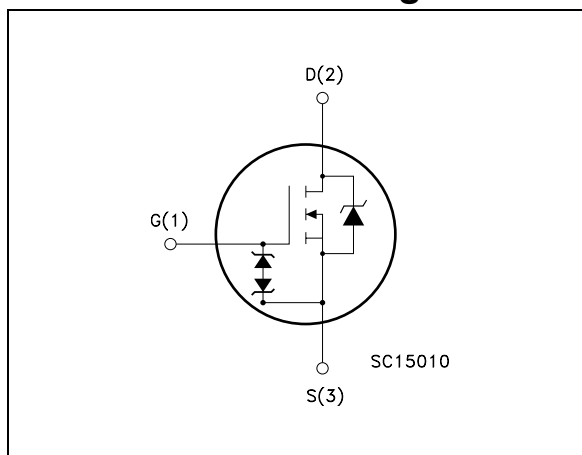
- Switching application



Order codes

Part number	Marking	Package	Packaging
STB9NK90Z	B9NK90Z	D ² PAK	Tape & reel
STF9NK90Z	F9NK90Z	TO-220FP	Tube
STP9NK90Z	P9NK90Z	TO-220	Tube
STW9NK90Z	W9NK90Z	TO-247	Tube

Internal schematic diagram



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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220/D ² PAK/ TO-247	TO-220FP	
V _{DS}	Drain-source voltage (V _{GS} = 0)	900		V
V _{DGR}	Drain-gate voltage (R _{GS} = 20KΩ)	900		V
V _{GS}	Gate-source voltage	± 30		V
I _D	Drain current (continuous) at T _C = 25°C	8	8 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C =100°C	5	5 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	32	32 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25°C	160	40	W
	Derating Factor	1.28	0.32	W/°C
Vesd(G-S)	G-S ESD (HBM C=100pF, R=1.5kΩ)	4		KV
dv/dt ⁽³⁾	Peak diode recovery voltage slope	4.5		V/ns
V _{ISO}	Insulation withstand voltage (DC)	--	2500	V
T _J T _{stg}	Operating junction temperature Storage temperature	-55 to 150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. I_{SD} ≤ 0A, di/dt ≤ 200A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ T_{JMAX}

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		TO-220 D ² PAK	TO-20FP	TO-247	
R _{thj-case}	Thermal resistance junction-case Max	0.78	3.1	0.78	°C/W
R _{thj-a}	Thermal resistance junction-ambient Max	62.5		50	°C/W
T _l	Maximum lead temperature for soldering purpose	300			°C

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _J Max)	8	A
E _{AS}	Single pulse avalanche energy (starting T _J =25°C, I _d =I _{ar} , V _{DD} =50V)	300	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1mA, V_{GS} = 0$	900			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating} @ 125^{\circ}C$			1 50	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20V, V_{DS} = 0$			± 10	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100\mu A$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 3.6A$		1.1	1.3	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15V, I_D = 3.6 A$		5.75		S
C_{iss}	Input capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		2115		pF
C_{oss}	Output capacitance			190		pF
C_{rss}	Reverse transfer capacitance			40		pF
$C_{oss \text{ eq}}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0V \text{ to } 720V$		115		pF
Q_g	Total gate charge	$V_{DD} = 720V, I_D = 8A$		72		nC
Q_{gs}	Gate-source charge	$V_{GS} = 10V$		14		nC
Q_{gd}	Gate-drain charge	(see Figure 19)		38		nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%
2. $C_{oss \text{ eq}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise Time	$V_{DD}=450\text{ V}$, $I_D=4\text{ A}$, $R_G=4.7\Omega$, $V_{GS}=10\text{ V}$ (see Figure 20)		22 13		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD}=450\text{ V}$, $I_D=4\text{ A}$, $R_G=4.7\Omega$, $V_{GS}=10\text{ V}$ (see Figure 20)		55 28		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD}=720\text{ V}$, $I_D=8\text{ A}$, $R_G=4.7\Omega$, $V_{GS}=10\text{ V}$ (see Figure 20)		53 11 22		ns ns ns

Table 7. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}^{(1)}$	Gate-Source Breakdown Voltage	$I_{GS}=\pm 1\text{ mA}$ (Open Drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				32	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=8\text{ A}$, $V_{GS}=0$			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=50\text{ V}$, $T_j=150^\circ\text{C}$		950 10 21		ns μC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220/D²PAK

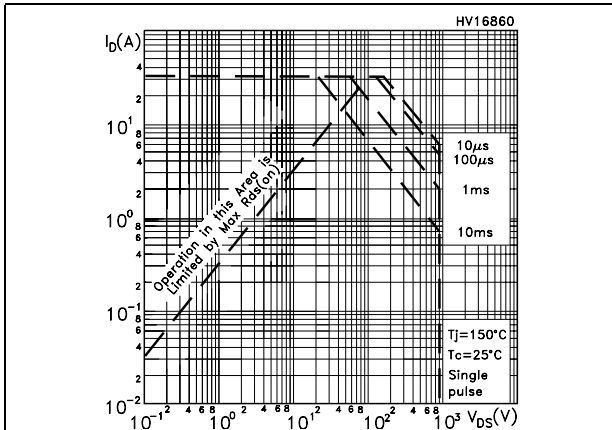


Figure 2. Thermal impedance for TO-220/D²PAK

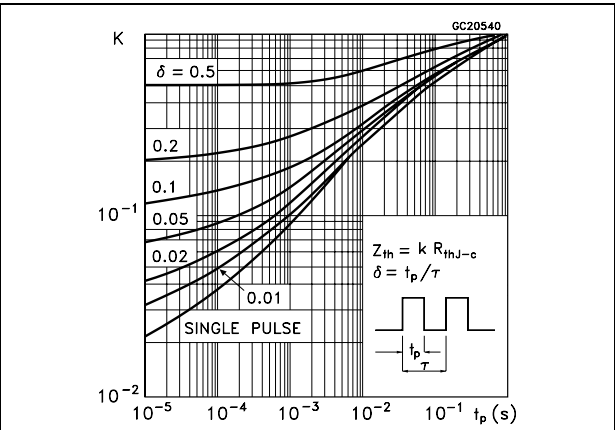


Figure 3. Safe operating area for TO-220FP

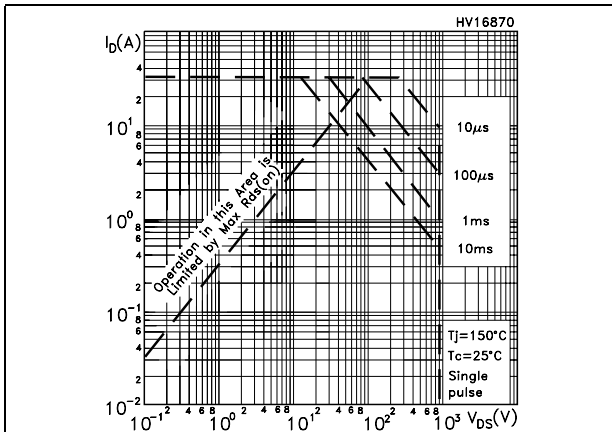


Figure 4. Thermal impedance for TO-220FP

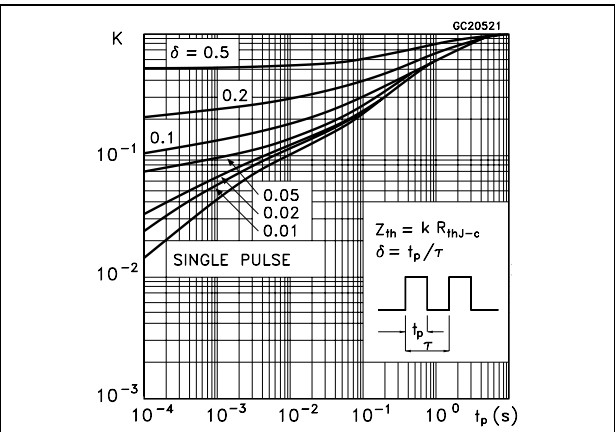


Figure 5. Safe operating area for TO-247

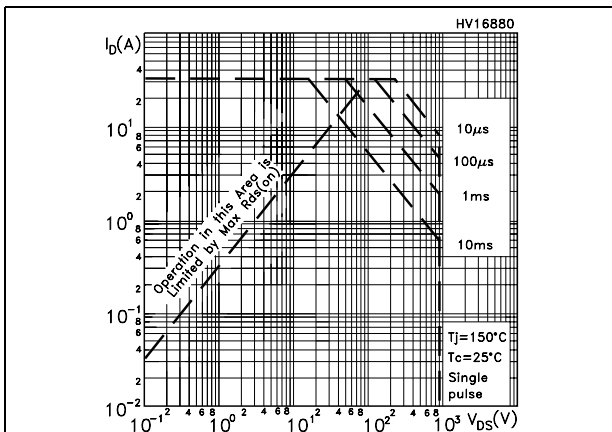


Figure 6. Thermal impedance for TO-247

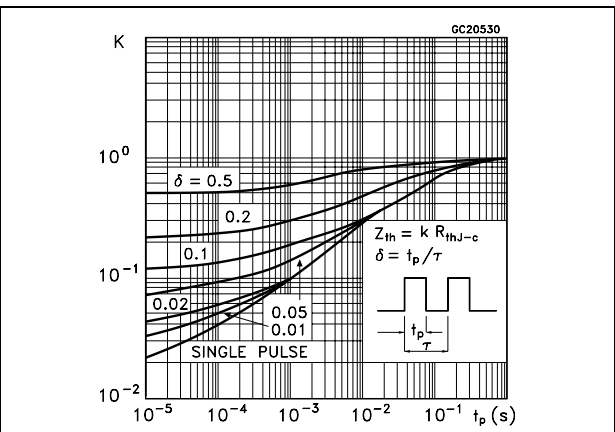


Figure 7. Output characteristics

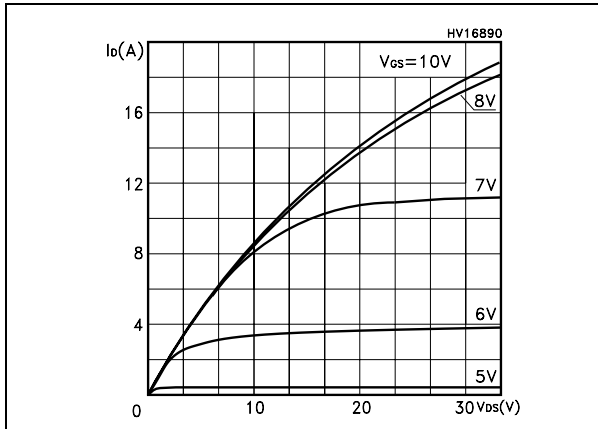


Figure 8. Transfer characteristics

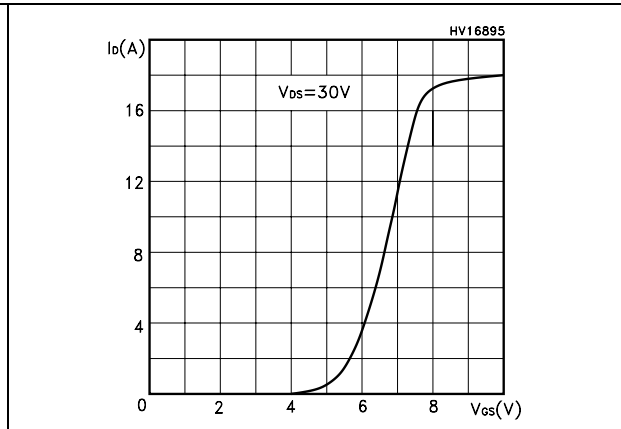


Figure 9. Transconductance

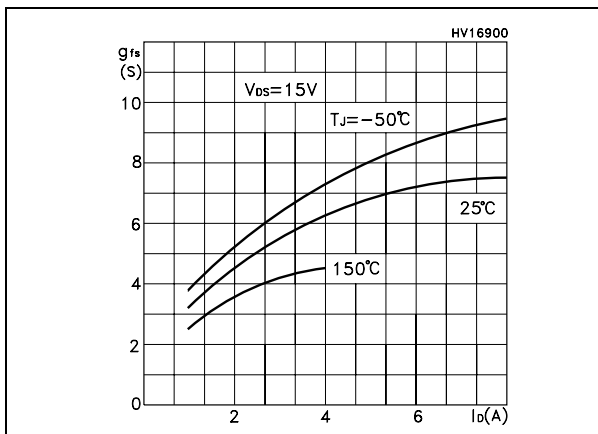


Figure 10. Static drain-source on resistance

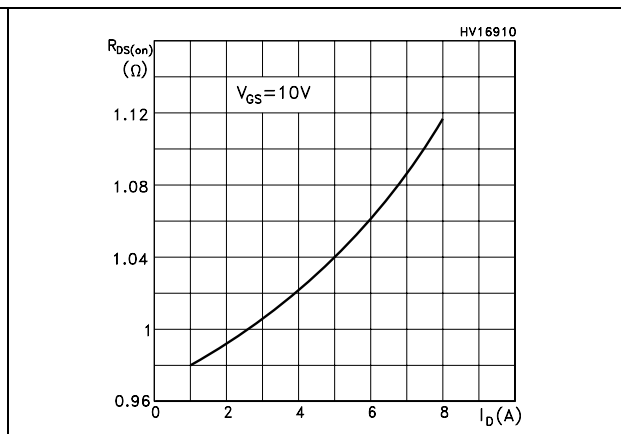


Figure 11. Gate charge vs gate-source voltage Figure 12. Capacitance variations

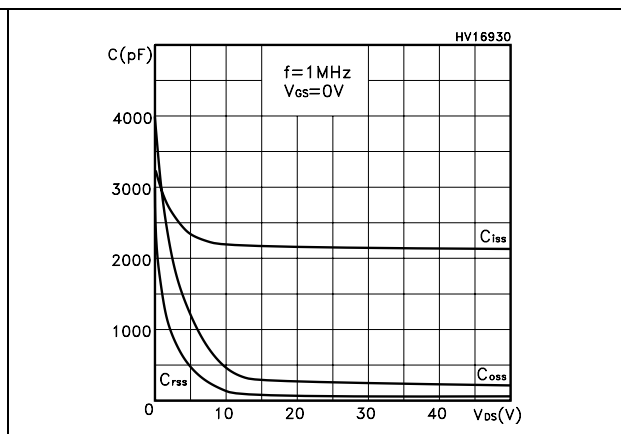
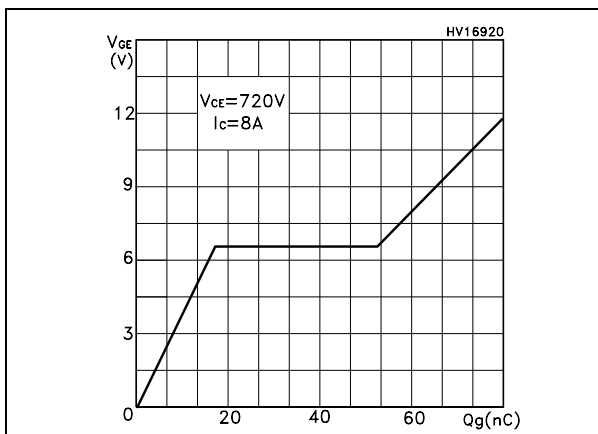


Figure 13. Normalized gate threshold voltage vs temperature

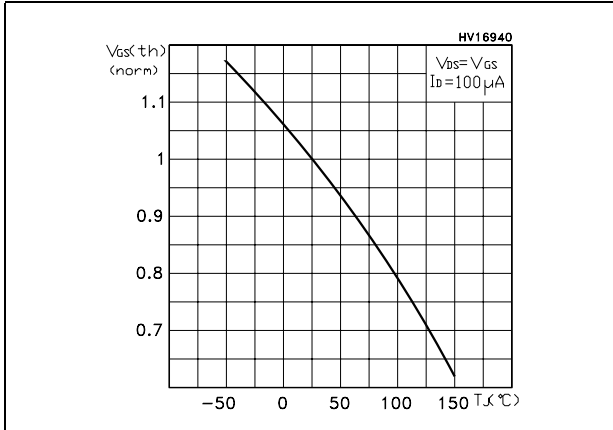


Figure 14. Normalized on resistance vs temperature

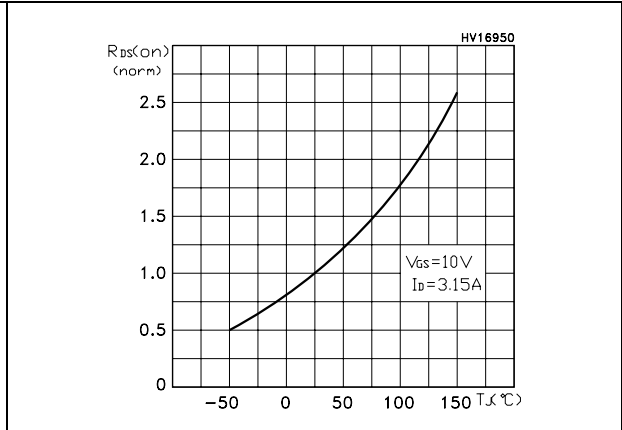


Figure 15. Source-drain diode forward characteristics

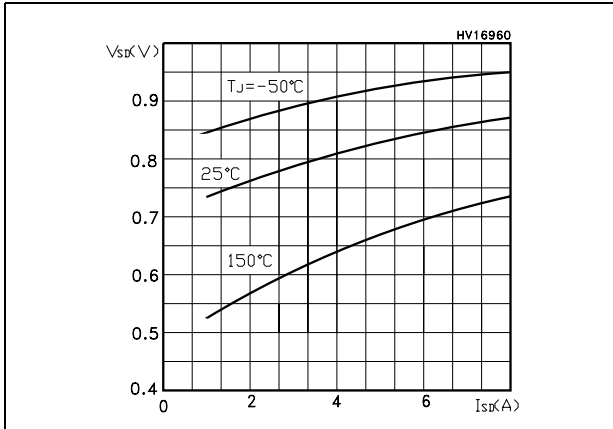


Figure 16. Normalized $B_{V_{DSS}}$ vs temperature

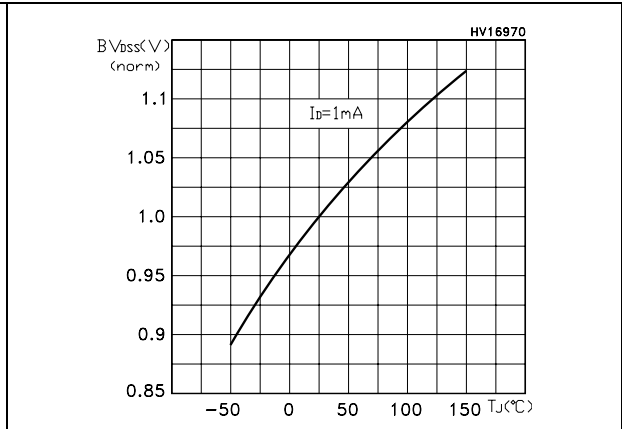
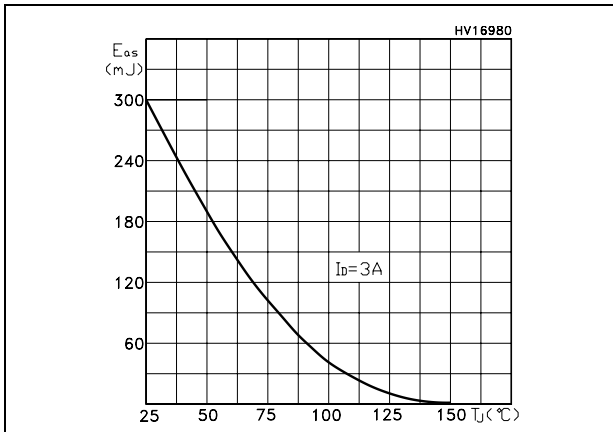


Figure 17. Maximum avalanche energy vs temperature



3 Test circuit

Figure 18. Switching times test circuit for resistive load

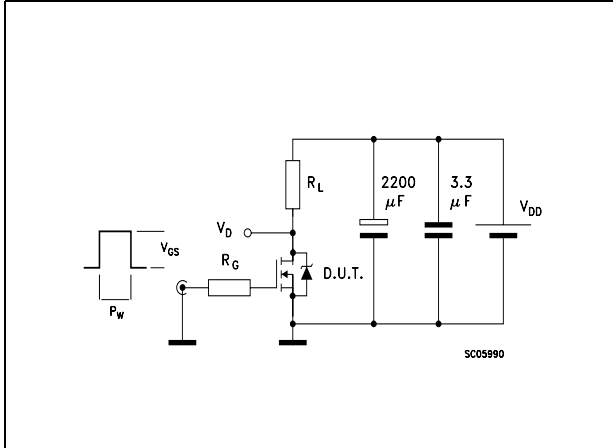


Figure 19. Gate charge test circuit



Figure 20. Test circuit for inductive load switching and diode recovery times



Figure 21. Unclamped Inductive load test circuit



Figure 22. Unclamped inductive waveform



Figure 23. Switching time waveform

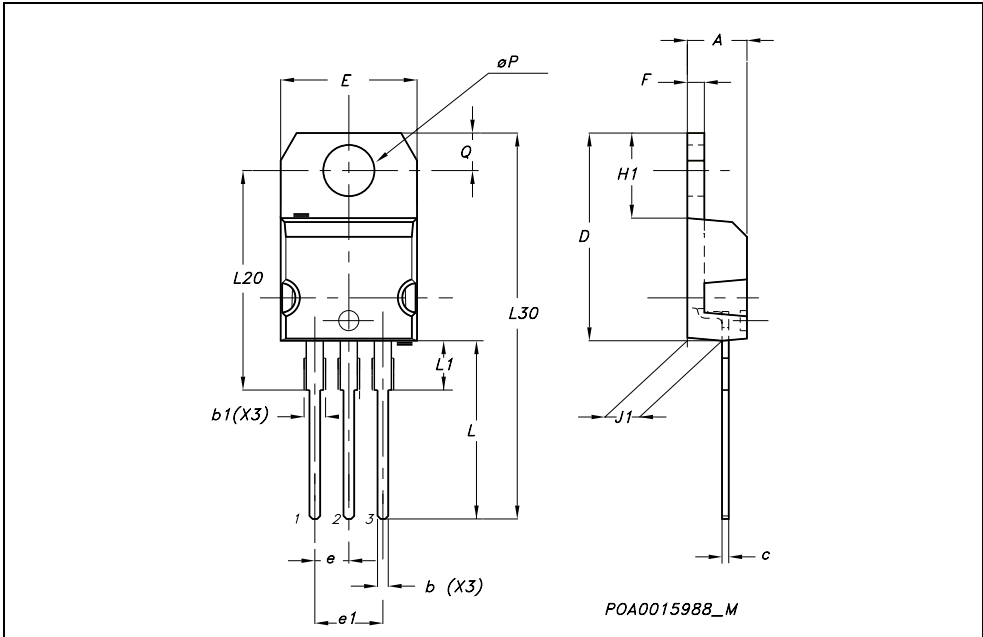


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

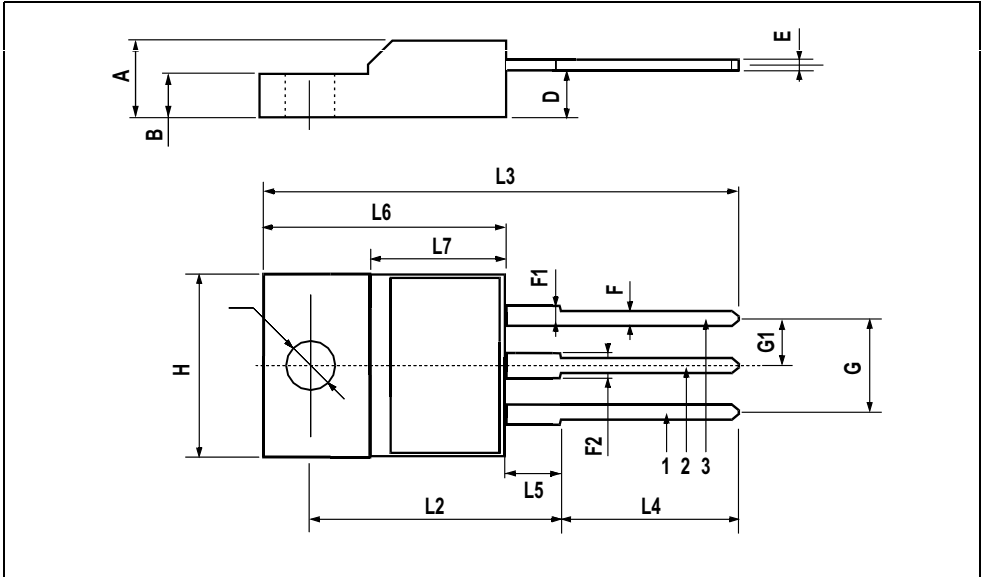
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



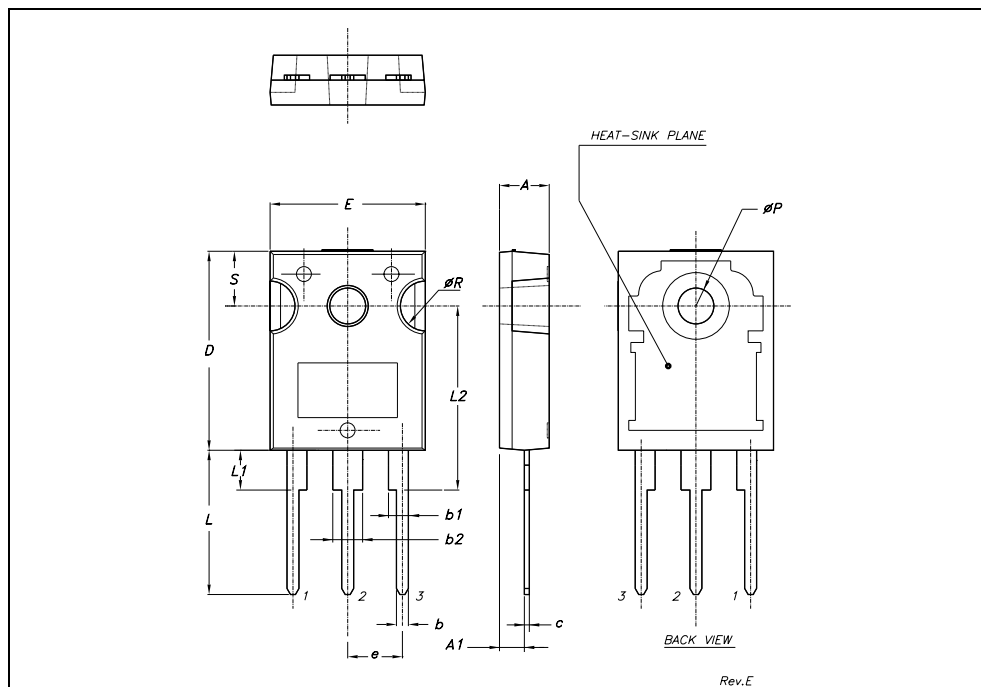
TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



5 Packaging mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

10 pitches cumulative tolerance on tape +/- 0.2 mm

Center line of cavity

User Direction of Feed

FEED DIRECTION

Bending radius R min.

* on sales type

6 Revision history

Table 9. Drevision history

Date	Revision	Changes
08-Sep-2005	2	Complete version
27-Oct-2005	3	Inserted ecopack indication
20-Jul-2006	4	New template, no content change

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